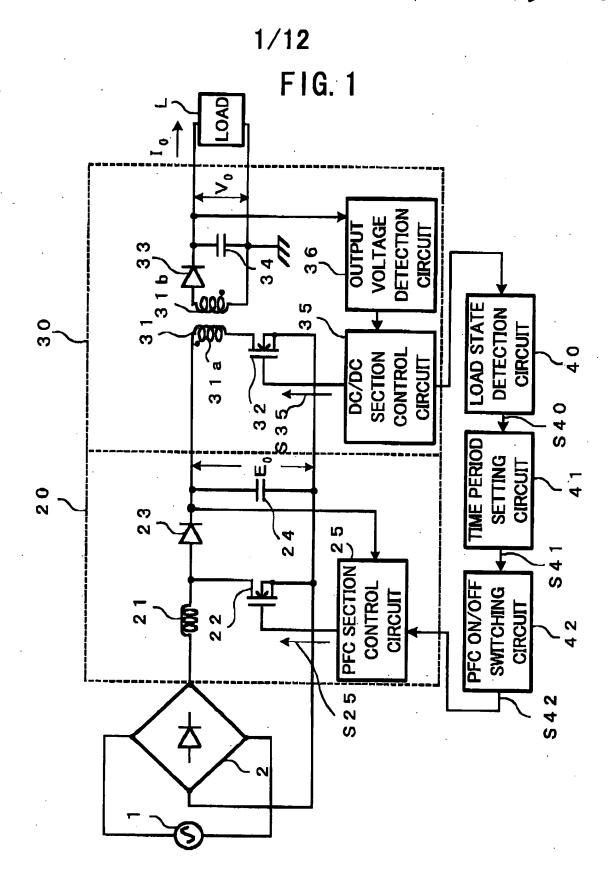
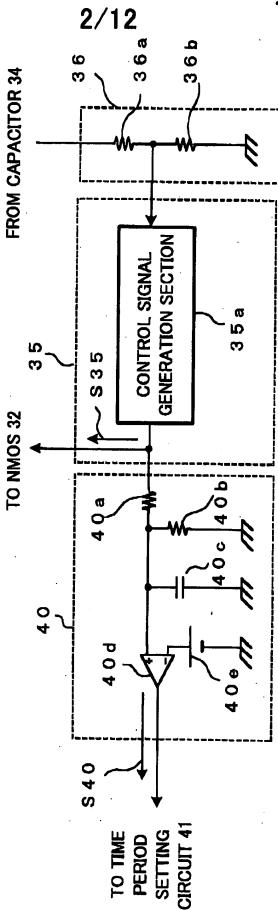
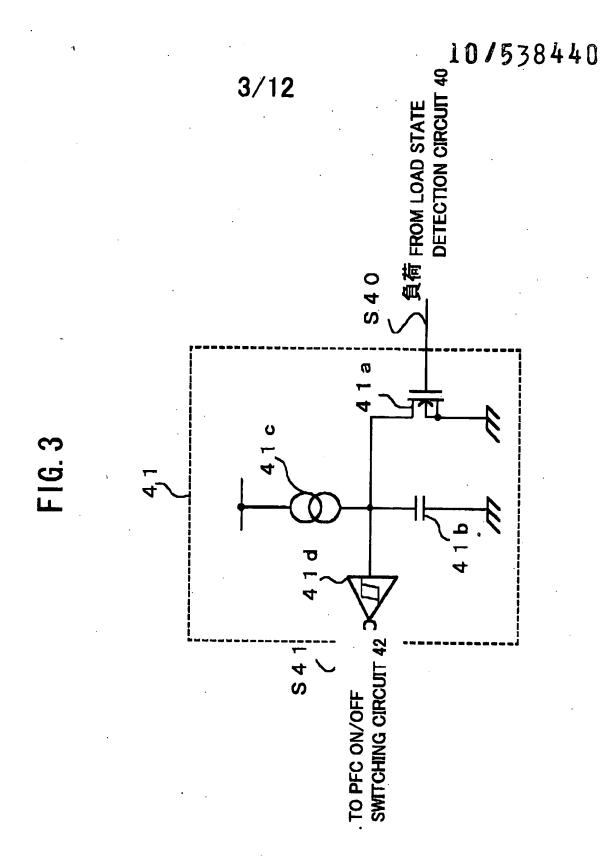
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10/538440



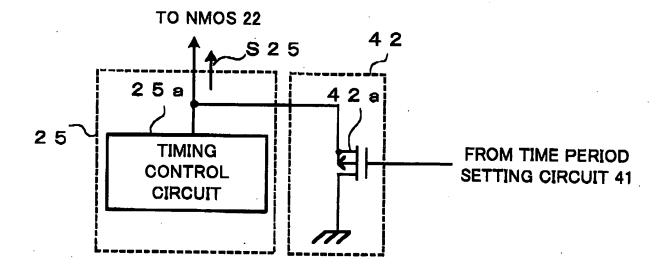
-IG 2



10/538440

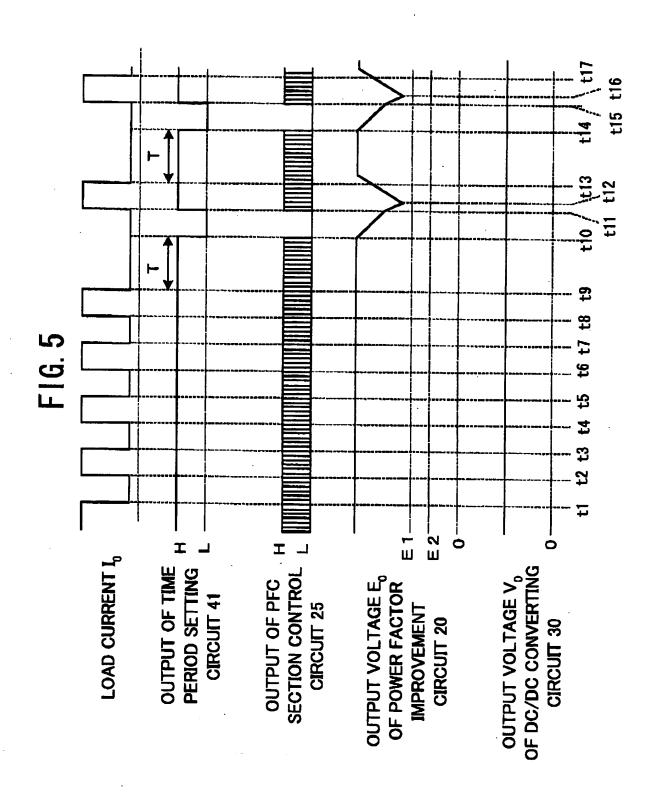
4/12

FIG.4

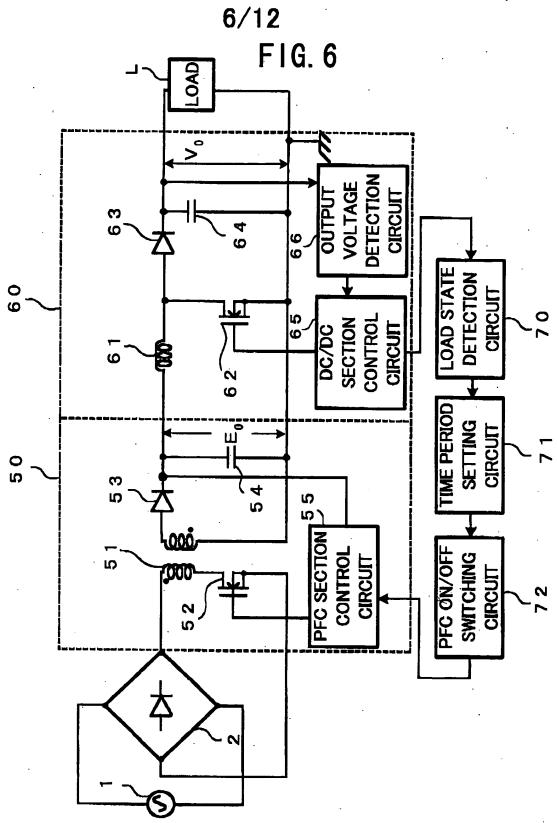


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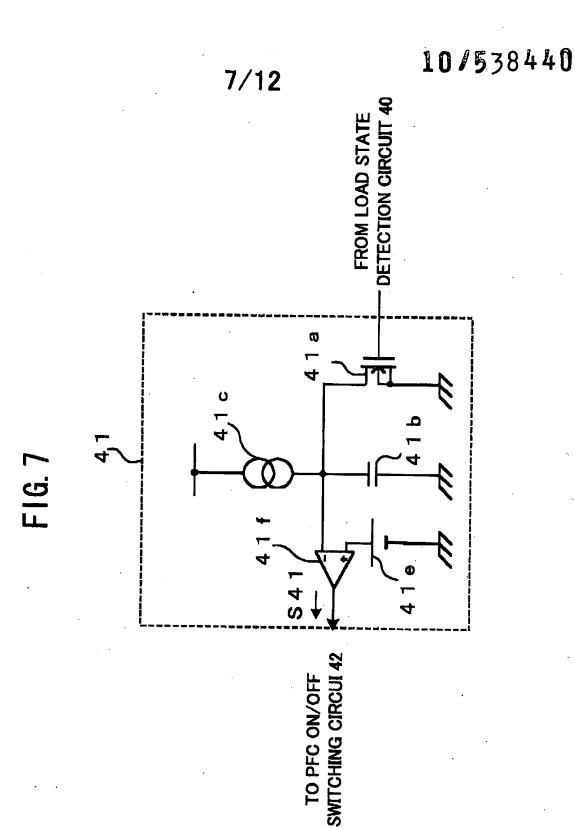
5/12



10/538440



3



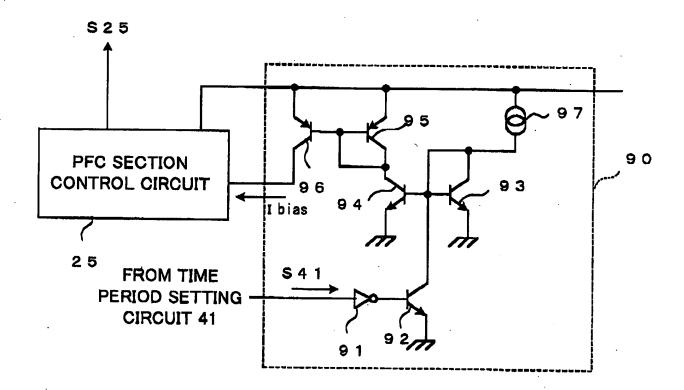
10/538440 FROM DC/DC SECTION CONTROL CIRCUIT 35 8/12 8 0 A S 3 5 O O TO NMOS 32 F16.8 8.4 a 84 P 08 8 4 PERIOD GENERATING SECOND REFERENCE PERIOD GENERATING FIRST REFERENCE CIRCUIT CIRCULT 80B 83 & 2 \

2 10

9/12

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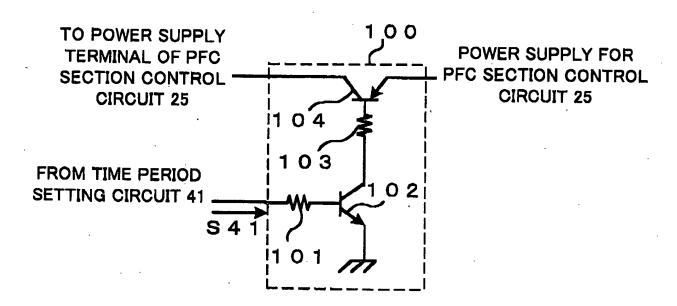
FIG. 9



10/12

10/538440

FIG. 10



10/538440

FIG. 12

